ABSTRACT

A processor has an architecture that provides the processing speed advantages of the Harvard architecture, but does not require two separate external memories in order to expand both data memory and program instruction memory. The processor has separate program memory space and data memory space, but provides the capability to map at least a portion of the program memory space to the data memory space. This allows most program instructions that are processed to obtain the speed advantages of simultaneous program instruction and data access. It also allows program memory space and data memory space to be expanded externally to the processor using only one external memory device that includes both program instructions and data. The processor includes a program memory space operable to store program instructions and data, a data memory space operable to store data, and mapping circuitry operable to map at least a portion of the program memory space to the data memory space. The program memory space may be internal to the processor. The processor may further comprise a page register operable to specify a location of the program memory space that is mapped to the data memory space.